ARMY RESEARCH LABORATORY

Foundation of a Heterogeneous Electronics Integration Platform

by Scott Trocchia, Dr. Christopher D. Meyer, Dr. Sarah Bedair, Dr. Tony Ivanov, Dr. William Benard, and Dr. Alma Wickenden

ARL-TR-6008 **May 2012**

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14. ABSTRACT

Due to increasing complexity, multi-material incompatibilities, and size constraints of electronics, no single monolithic technology can adequately realize the full spectrum of Army-relevant applications. The integration of a wide range of devices, each fabricated in different technologies and performing a well-defined task, would enable the construction of high performance systems. We use a custom microfabrication process flow to align dies within a silicon template wafer to obtain a common planar surface between them. The resulting silicon wafer with embedded chips would then be compatible with the U.S. Army Research Laboratory's (ARL) high quality factor (Q), state-of-the-art multilevel copper electroplating process. This approach permits high density interconnects and through silicon vias, reduces pad parasitics and allows researchers to construct highly miniaturized, modular heterogeneous platforms for Army systems. Future work will include testing and characterization of prototype heterogeneously integrated designs.

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1. Introduction/Background

1.1 Defining Heterogeneous Integration

The fabrication and processing of dissimilar components onto one common substrate (monolithic integration) is often not practical due to material and thermal processing incompatibilities. Heterogeneous integration represents a strategy to alleviate these constraints. Heterogeneous integration is a technique whereby components are each fabricated separately in compatible technologies, diced into individual chips, and then interconnected with other chips fabricated in different technologies on one common substrate, as illustrated in figure 1. This strategy combines the high density features of monolithic (single substrate) integration with the advantages of hybridization—chips are fabricated in individual technologies that are ideally suited to yield the best performance. Heterogeneous integration can be realized through a number of different methods that can broadly be categorized into chip- and wafer-level integration. Wafer-level integration has the advantage that the integration processes are performed in batch on many copies of a particular system at once, in contrast to the serial, part-by-part processing of chip-level integration.

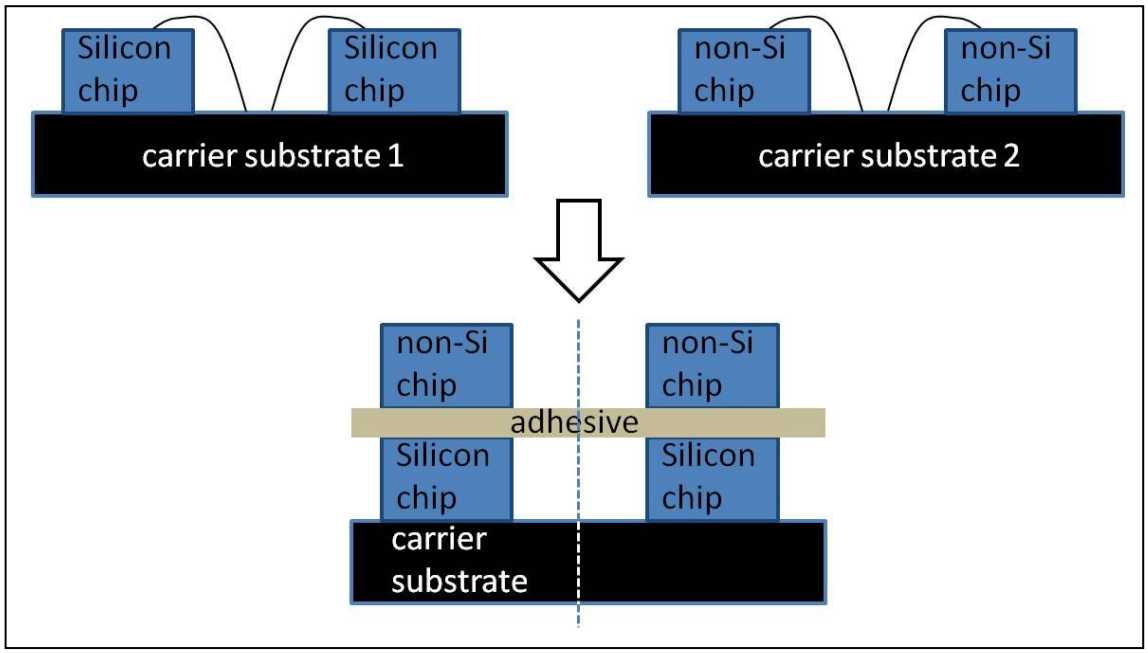


Figure 1. Heterogeneous integration.

1.2 Motivation

The objective of this work is to enable the heterogeneous attachment of multiple arbitrary die, or chips, into one streamlined, higher-order two-dimensional platform (figure 2). A system as a whole can benefit by receiving a high performance boost if disparate chips, each adept at performing different tasks, co-operate.

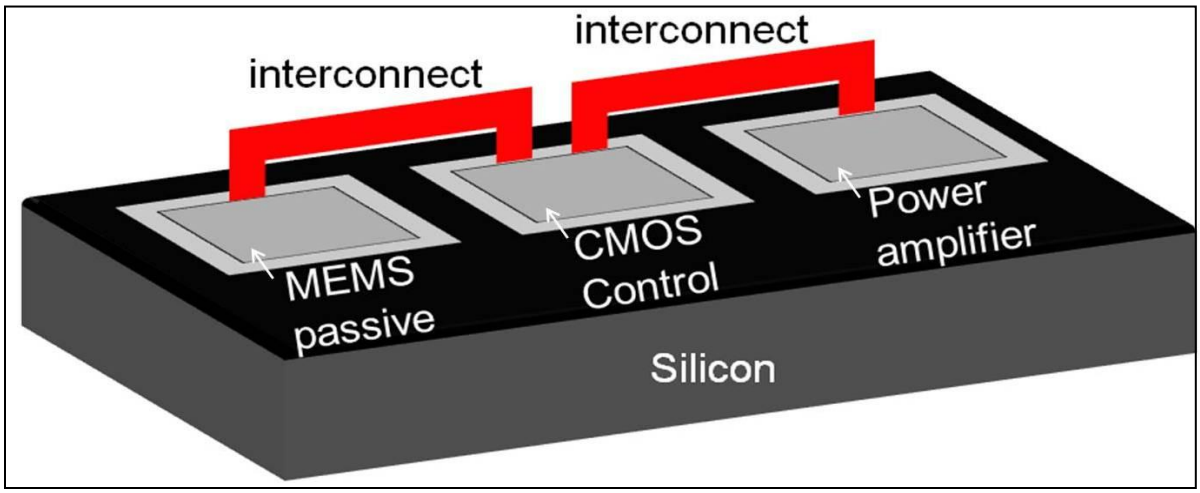


Figure 2. Streamlined heterogeneous integration platform composed of disparate chips.

A heterogeneous architecture is essential for the advancement of technology and for a wide array of Army technologies, including, but not limited to, communications, robotic, and distributed power platforms. This attitude is part of a philosophy commonly referred to as "extending Moore's Law" or "More than Moore" (*3*).

In this project, we seek to create compact systems composed of different die performing different, unique tasks. Multiple die are aligned within a silicon template wafer and planarized to enable the construction of electrical interconnects on various layers. The concepts of bulk micromachining the silicon wafer and realizing a unified system with high-density interconnects are tested.

2. Process Flow

We customize an existing microfabrication routine for silicon (Si)-based technologies and expand upon it to cater to our trench-based design. The steps that we employ can be summarized as follows:

- Create cavities in a Si template by deep reactive ion etching (DRIE).
- Bond template wafer to blank backing wafer.
- Place die into template wafer with frontside contacting blank wafer for planarity.
- Electroplate to fill the trenches and lock the die in place.
- Detach the blank wafer.

Figure 3 illustrates the sequence in its entirety. First, we start with a bare 100-mm-diameter silicon wafer, Silicon wafer #1, which is to serve as the template wafer. After thoroughly cleaning the wafer with acetone, methanol, and isopropyl alcohol, we spin a thin layer of AZ9245 positive photoresist on top to mask portions of the wafer from being etched during DRIE. Our photoresist process flow (figure 3a) used a conventional implementation of cleaning, coating, soft-baking, exposure, development, and post-exposure hard-baking (PEB).

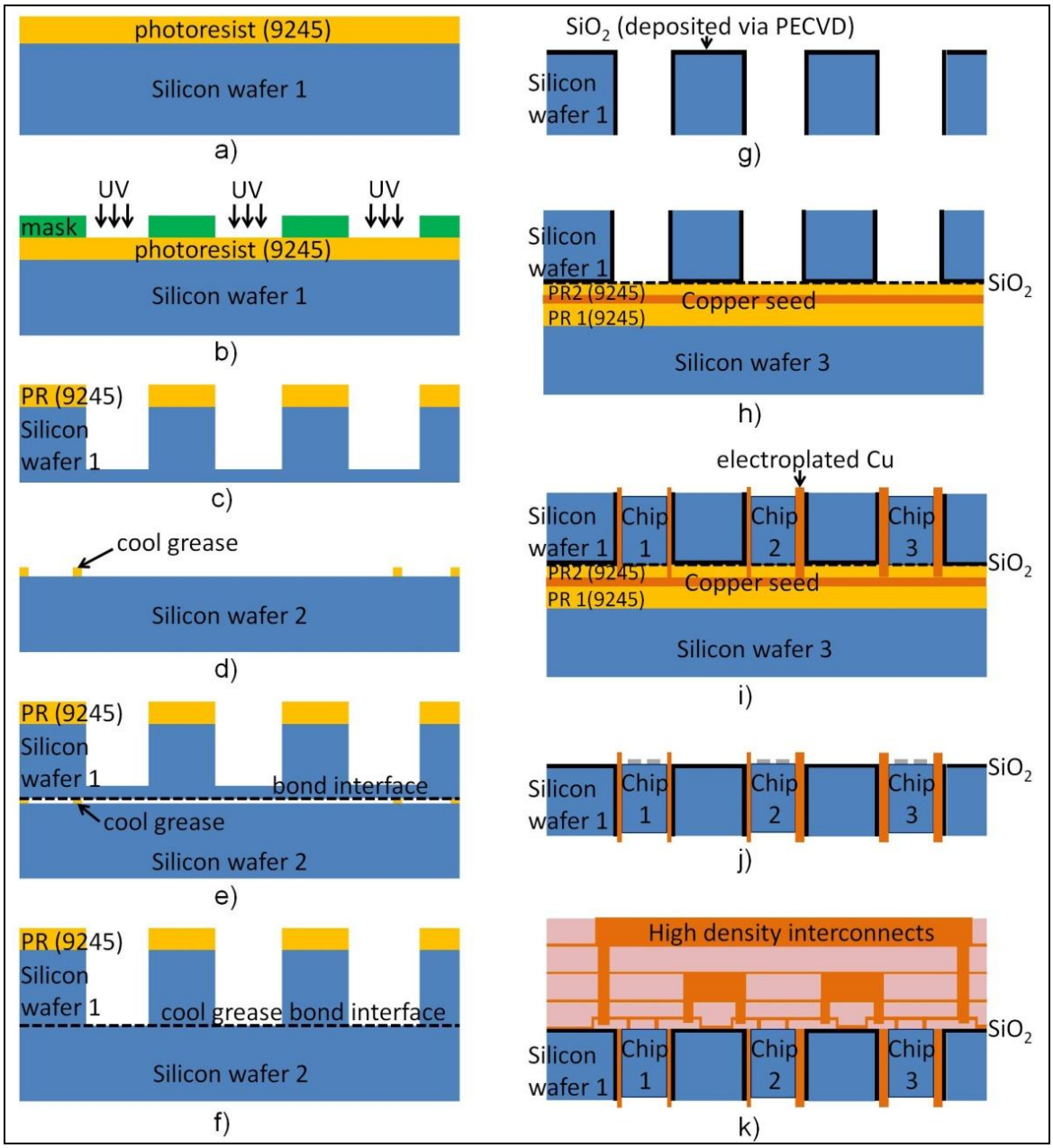


Figure 3. Three-wafer fabrication and processing of trenches: (a) photoresist deposition, (b) soft mask exposure and development, (c) partial DRIE of trenches, (d) Cool-Grease™ application, (e) hot plate wafer bond, (f) DRIE completion, (g) detach wafer and oxide deposition, (h) re-attach wafer, (i) trench copper (Cu) electroplating, (j) detach and flip single wafer over, and (k) layer Cu electroplating.

A customary soft-bake is executed in an oven to evaporate solvents in the resist. Unwanted resist around the wafer's perimeter is removed through an edge bead removal (EBR). Later on in the process sequence, the mechanical clamps of the DRIE tool should tightly grasp the pure Si edge of the wafer without interference from other substances. A separate soft-bake is performed to remove excess solvents created by resist splattering during EBR. Lastly, the wafer is submerged in water to rehydrate the resist. Typically, rehydration is done before any exposure procedure because the photoresist development requires water content in the resist film. The end result is a pristine, planar surface of AZ9245 photoresist coating on the surface of Silicon wafer #1.

This photoresist coating is then exposed to ultraviolet (UV) light that is masked through a chromed glass plate containing the pattern to be transferred to the photoresist. After exposing the photoresist to UV light and developing in AZ400K developer 1:4—one part of developer to four parts of de-ionized (DI) water—the pattern appears as exposed regions of photoresist are in the developer. During development, one should manually agitate the liquid to facilitate the development procedure. Residues are removed through a subsequent O_2 plasma process (de-scum).

The resulting single template wafer (Silicon wafer #1 in figure 3c) is ready to undergo the DRIE Bosch process. Through a subtractive procedure, the Bosch process etches high aspect ratio cavities. As visualized in figure 4, the reaction of two separate gas chemistries, sulfur hexafluoride (SF_6) and octafluorocyclobutane (C_4F_8), is time-multiplexed in a vacuum chamber. Applied radio frequency (RF) signals trigger the release of these two gases. At one time instant, the first gas etches the Si; at the next time instant, the second gas, through low-temperature plasma-enhanced chemical vapor deposition (PECVD), conforms to the sidewalls of the growing cavity, resulting in a higher etch rate vertically than horizontally. These two steps iterate until the proper depth is achieved. Table 1 lists the characteristics of a conventional Bosch process.

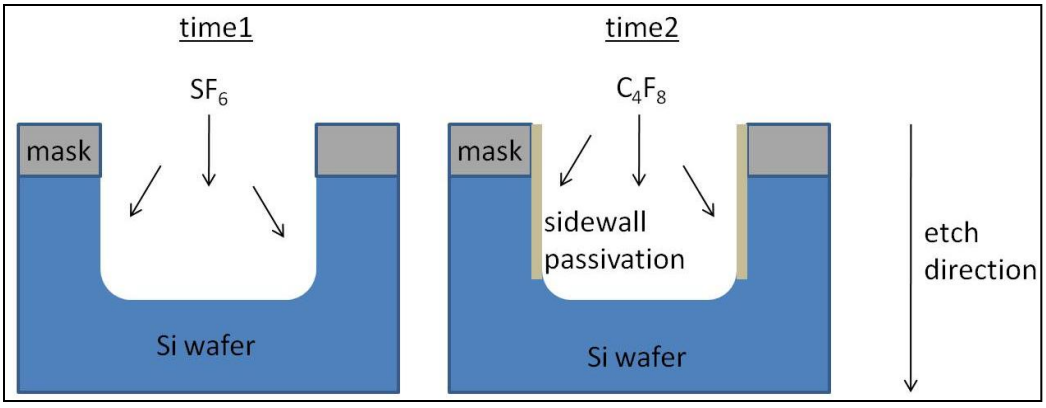


Figure 4. Visualizing alternative Bosch process steps.

Table 1. Process characteristics for conventional Bosch process.

SF_6 flow	30–150 standard cubic centimeters per min
C_4F_8 flow	20–100 standard cubic centimeters per min
Etch cycle	5–15 s
Deposition cycle	5–12 s
Pressure	0.25–10 Pascals
Temperature	20–80 °C
Etch rate	1.5–4 μm/min (higher than RIE etching)
Sidewall angle	90° ± 2°
Selectivity to photoresist	150 to 1
Selectivity to SiO_2 hard mask	over 300 to 1

The patterned trenches are partially etched to the point where 5–10% of the original Si thickness remains to be etched to prevent backside helium cooling gas from leaking into the frontside etch chamber. When the DRIE occurs, the only parts of the trench being etched are the narrow 500-micron moats/crevices surrounding the interior square; once that process completes, the interior square falls out because it does not have a contact point on which to grip. Square trenches with labeled dimensions (in mm) and near-vertical sidewalls are produced.

After the initial etch, the template wafer is bonded with Cool-Grease to a backing wafer in order to continue etching entirely through the template wafer. Cool-Grease is the bonding agent of choice due to its higher thermal conductivity over other adhesive options such as AZ9245 photoresist (4.04 W/m-K compared to 0.2 W/m-K). A few drops of Cool-Grease™ are applied to four periphery locations on the carrier, and the template is loosely lined up on top of Silicon wafer #2 (figure 3d). The stack is heated up to 55 °C and allowed to cool immediately thereafter (figure 3e).

Then, the formed stack is loaded back into the etch chamber so the DRIE can run to completion and produce nominal 500-μm-deep trenches within a 500-μm-thick wafer (figure 3f). The backing wafer, wafer #2, ensures that released Si features do not fall into the vacuum chamber, which is problematic for subsequent equipment operation. Individual interior squares are removed with tweezers. No longer needed, the Cool-Grease™ bond is broken by twisting the two wafers in opposite directions and allowing wafer #1 to slide away from wafer #2. None of the features are tampered with and the Cool-Grease™ continues to function as a paste at this temperature.

A thin-film of silicon dioxide (SiO_2) is deposited via PECVD on the template, which is now detached and only consists of pure silicon (figure 3g). The 100-nm oxide coats the trench sidewalls and the exposed top surface of the wafer. A color chart relays quantitative experimental data of color versus thickness deposited. This layer can serve as passivation so that electroplated Cu will not electrically short to the bulk Si.

Two 100-mm-diameter wafers have been used in the fabrication process up to this point—the patterned template wafer, Silicon wafer #1, and one carrier wafer, Silicon wafer #2. A third wafer is then coated with a three-layer stack consisting of photoresist, sputtered coper (Cu), and another layer of photoresist. This third wafer (Silicon wafer #3), acting as a carrier wafer and also providing the Cu seed onto which Cu will be electroplated in the trenches between the chips and the template wafer, is bonded at room temperature to the underside of the template; a connection between PR2 (labeled in figure 3h) and the unpolished side of the Si template wafer results. All ensuing parts of the fabrication process are constructed upon this two-wafer stack, and the height of the structure never reaches more than two wafers (plus the intermediate bonding layers). Arbitrary die/chips are manually placed, face down, via a pick-and-place approach at room temperature and allowed to rest on the photoresist base (PR2), with all electrical pads in contact with the PR2 layer.

The wafer bundle is subjected to a hot plate temperature of 110 °C at which the PR2 is adhesive enough for the chips to be lightly pushed down and secured in place. The embedding of chips is crucial, for the trench is a pattern guiding the chip alignment. A more sophisticated pick-and-place tool could be used for higher resolution alignment accuracy. Additionally, by placing chips into a planar bed of photoresist, we ensure that the chips will be offset from the frontside of the wafer by a distance smaller than or equal to the resist thickness. Planarity is a major critical detail of our fabrication sequence in order to enable microfabrication of high-density interconnects on the frontside of the wafer.

Almost fully assembled—from bottom to top: carrier, thick AZ9245, seed, thinner AZ9245, and template plus chips—the stack is dropped into a water bath to rehydrate the top resist (PR2). The top wafer is exposed to UV light and developed in AZ400K developer. Remaining residues are removed through a de-scum process.

A sulfuric acid (H_2SO_4) bath is prepared for the plating process. This electroplating bath, illustrated in figure 5, is composed of H_2SO_4 and DI water. A rectangular Cu plate—representing the anode—is immersed at one end of the bath and connected to a positive external voltage; the wafer to be electroplated—representing the cathode—is electrically grounded. When subjected to an applied voltage, Cu^{2+} ions are excited and move from a region of higher potential (anode) to a lower potential surface area (cathode); the source current determines the plating rate. The aforementioned ions gain two electrons in their valence shell, thus forming neutral Cu, and begin to plate onto the wafer’s surface.

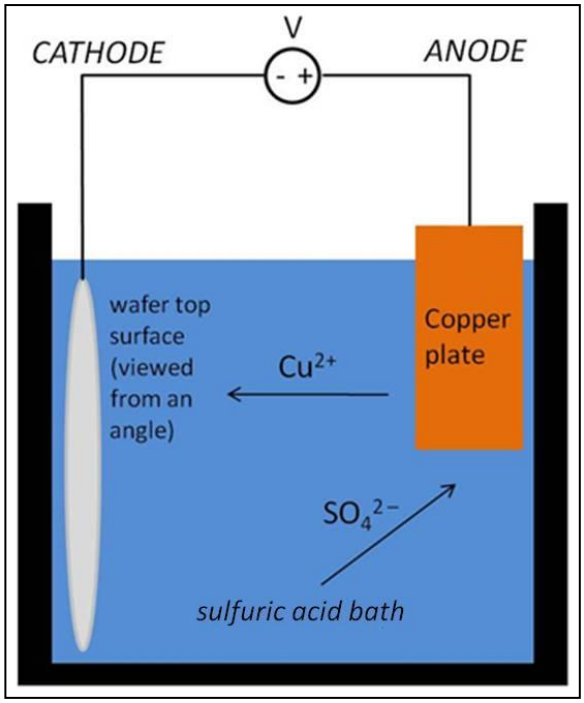


Figure 5. Cu electroplating bath setup.

Vertically oriented with the features of the wafer facing into the bath, the wafer stack is fully submerged in the solution. Plating occurs because metal clips are in contact with the Cu seed on the wafer, allowing a continuous electron flow to occur. The plating rate is (1) heavily influenced by the current density over a fixed plating surface area and (2) controlled by maintaining a fixed current for a measured time period. The fluid in the bath, consisting of transient Cu and sulfate ions, wicks into the channels and allows Cu to grow upward. Multiple Cu pillars are needed to mechanically connect the chip's edges to the trench's sidewalls and to create through-Si-vias (TSVs) for further electrical connections.

Once the wafer trenches have been plated most of the way through, Silicon wafer #3 is detached on a hot plate; the template wafer, with blank die and Cu vias intact, is pushed away from the carrier (wafer #3). Removal via acetone or Baker's PRS-3000 is not essential, although it is possible. However, because the solvent must flow into narrow, high aspect ratio channels containing resist—100 mm across versus 10 μm thick—chemical removal takes longer.

3. Results and Discussion

3.1 Through Wafer Etch Tests

By creating trenches in three distinct template wafers, we were able to characterize etch rates for a through-wafer DRIE Bosch process; these measurements were experimentally determined

using a stylus profilometer. Each etch depth was recorded in a wide location where the triangular tip of the profilometer would not come in contact with the trench sidewalls, thereby limiting its chances of breaking. Table 2 details the measured etch rates for three separate wafers. The initial wafer thicknesses, etch times, and etch depths are recorded, and the etch rates are calculated from that collected data.

Table 2. Cumulative wafer etch rate case study.

		Etch Times (min)		**Average Etch Depth (μm)**		**Etch Rates (μm/min)**	
	Starting Wafer Thickness (μm)	**Incremental**	**Total**	**Incremental**	**Total**	**Incremental**	**Total**
Wafer No.							
1	488	90	90	295	295	3.28	3.28
		30	120	87.7	382.7	2.92	3.19
		25	145	72.5	455.2	2.90	3.14
2	494	120	120	386	386	3.22	3.22
		25	145	68.3	454.3	2.73	3.13
3	506	150	150	466.5	466.5	3.11	3.11

Discrete etch rates slow down over time because the gas chemistries have to traverse into and out of deeper trenches. Thus, thicker wafers demand more etching time. Based upon the research conducted by Yeom et al. (*16*), this observation is rational: the etch rate should slow down from ~3 μm/min to 2.4 μm/min when the features to be etched decrease in width from 500 μm to 100 μm. Yeom concludes that increased loading effects, increased aspect ratio, and the use of a different etch recipe are some of the factors that likely contribute to this aspect ratio dependent etching.

These measurements only give an approximation of the average etch rate across the wafer. Yet, the results are consistent across one nominally 500-μm-thick wafer. A full etch results in a profile with evidence of some mask edge roughness and scalloping along the sidewalls (figure 6). This effect is expected for an iterative Bosch process.

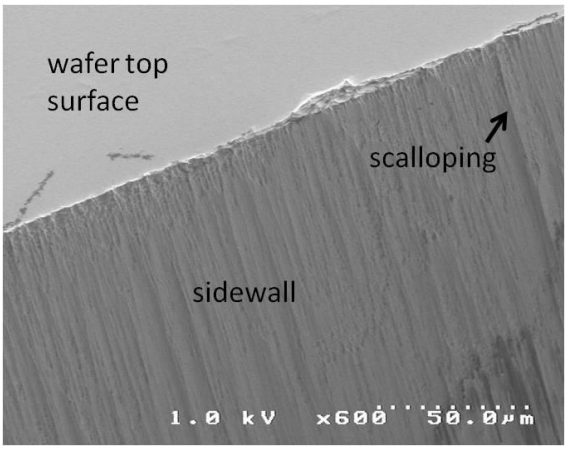


Figure 6. Mask edge roughness and sidewall verticality.

3.2 Photoresist Tests Performed

The fact that the photoresist may fully disappear before the through-wafer etch completes is of concern to us as well, leading to thinning of the template wafer itself. This thinning of the photoresist soft mask during DRIE was analyzed, and we used the interferometer to assess our measurements on two wafers. The same steps were used for both measurements. Still, due to wafer thickness variation in the DRIE, the results differ. Table 3 summarizes our findings.

Table 3. Photoresist etch rate and selectivity case study.

	Photoresist				**Wafer**	
	Starting Thickness (µm)	**Etch Time (seconds)**	**Average Etch Depth (µm)**	**Calculated Etch Rates (µm/min)**	**Etch Depth (µm)**	**Si-to-photoresist Selectivity**
Wafer #						
1	10	10000	4.5	.027	494	110:1
2	10.3	7200	4.7	.039	356	76:1

For our first wafer test, we started out with a fairly uniform thin photoresist layer. The etch rate in a time span of 2 h and 45 min (10,000 s) was 0.027 µm/min. In that same interval, 494 microns of Si in the center of the wafer were hollowed out; thus, the Si-to-photoresist mask selectivity exceeds 100–to–1. We carried out the same test with our next wafer and measured an etch rate of 0.039/min and a selectivity ratio near 75–to–1. Both quantities are comparable to our first trial run.

This gathered data proves that our selection of the photoresist mask thickness suffices. Despite that, a thick resist does outgas and crystallizes on the wafer's top surface in the etch chamber. To remedy this, after all of the lithography steps have been performed, we would hard-bake the template wafer to lessen the amount of gas the resist releases.

3.3 DRIE Bosch Process: Potential Pitfalls

The multiple through-wafer and photoresist tests we performed gave us insight into potential pitfalls in the process flow. Three interrelated issues are paramount:

- *Loss of helium compliance*—By etching through the wafer and not using a backing wafer, we run the risk of etching too far and losing helium compliance. The helium gas in the chamber would leak through the gaping openings in the substrate. The machine errors out and stops execution because it believes the thermal ground plane is lost. We noticed less uniformity across the wafer: some trenches broke through while others did not—the DRIE lag effect.
- *Loss of thermal ground plane*—The idea is to minimize thermal isolation between the template and the carrier/handle backing wafer so that heat can escape to a thermal ground plane. By mounting the template wafer too early in the process, the backing wafer adds its own thermal resistance to the system. Complicating that problem is the fact that the bonding agent is thermally variable and inconsistent from wafer to wafer, so different tests will inherently have different resistances associated with them. The selectivity of the photoresist to Si lessens with increasing wafer temperature, and the resist disappears before the through-wafer etch completes.
- *Filleting within the trenches*—In some of our trial runs, we failed to etch completely through the trenches, leaving residual Si ledges that jut out into the open areas of the trenches (figure 7). Problems arise because the so-called fillets block UV light from reaching the lower extremities of the trench, so the underlying resist will not get exposed and developed out in the figure 3i step. Consequently, we cannot guarantee that plating will occur in those regions; there is no direct access to the seed. Our proposed solution is twofold: either overetch to minimize the fillets, or use a double side polished (DSP) wafer and lithographically define our trenches on both sides of the wafer. In the second case, we would anisotropically etch from both sides of the wafer. The unwanted fillet would be pushed to the middle of the wafer. This methodology has not been tested, yet we recognize it is a robust solution to the filleting issue.

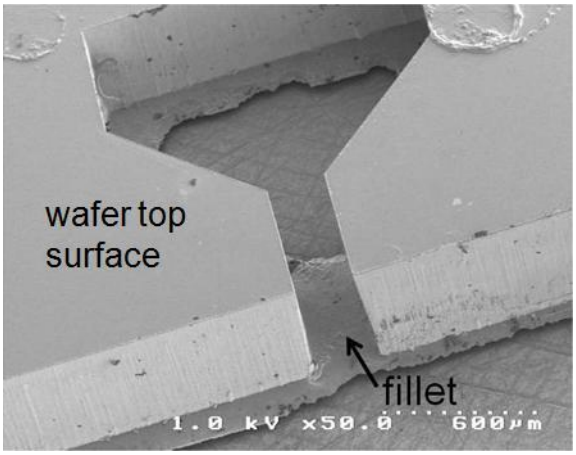


Figure 7. Filleting at the bottom of the trenches.

3.4 Amended Process Flow: Copper Seed Placement

After analyzing etch rates and optimizing the DRIE process, we focused on amending the process flow. Specifically, we hypothesized that by depositing a conformal seed on top of the chips and template wafer—rather than laying the seed first and then aligning the chips in the template, as is outlined in section 2—we can prevent chips from delaminating from the photoresist and, therefore, improve yield. Figure 8 describes this alteration. Advantages include the electrolyte has easier access paths to flow onto the seed and the seed conforms to the wafer shape. Conversely, a disadvantage is noted: there is the possibility that the seed is discontinuous and will not reach the bottom of the trenches, thereby undermining the structural planarity on the frontside. This concern exists with the first sputtering approach as well.

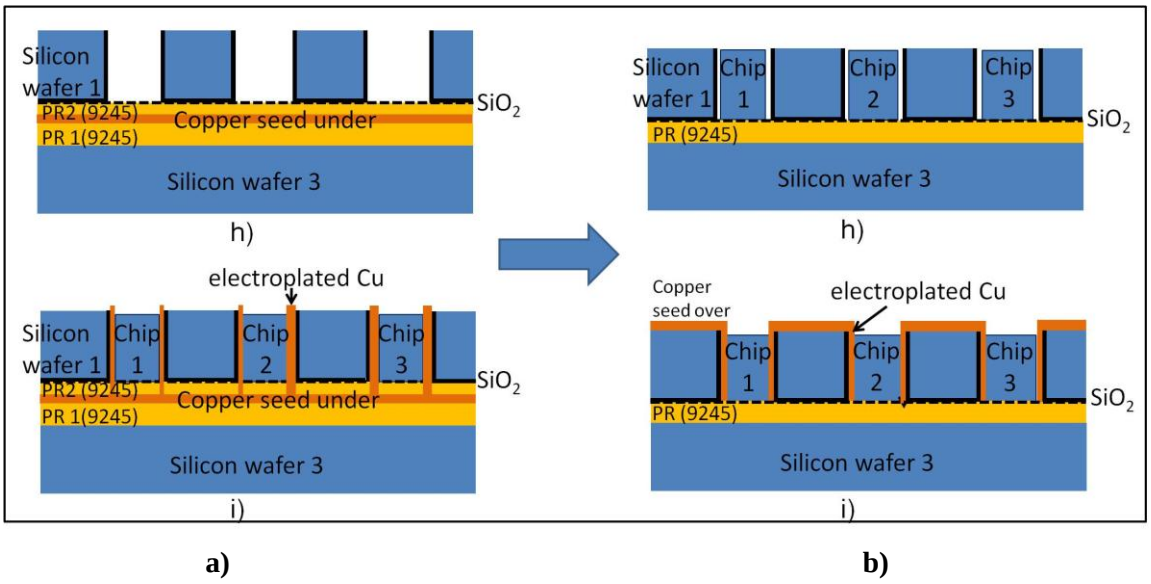
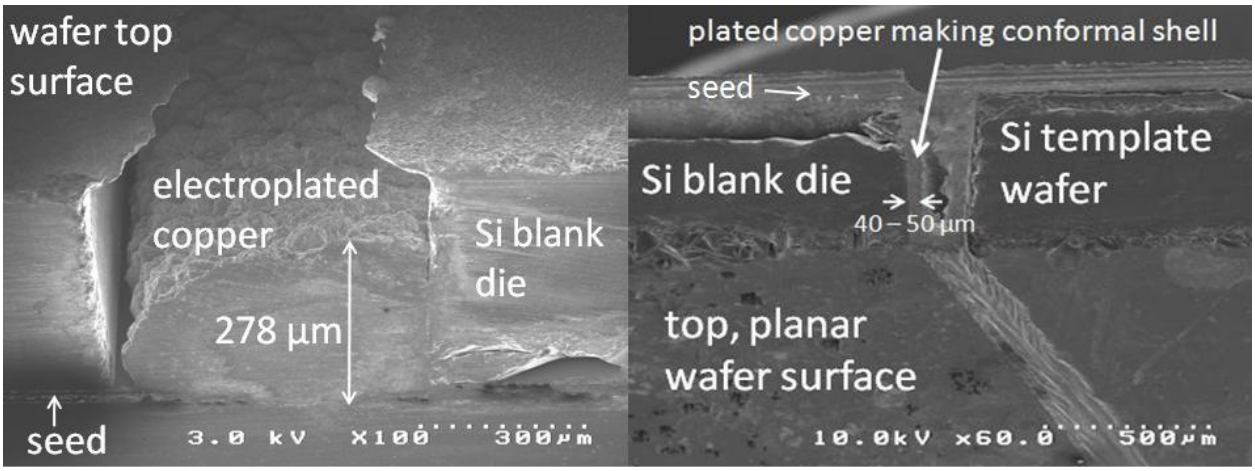


Figure 8. Amended process flow steps to account for Cu seed placement: (a) underneath the template and (b) on top of the template.

Scanning electron microscopy (SEM) images illustrate that a plated wafer with the Cu seed sputtered before the chips were placed (described in the process flow illustrated in figure 3) yields Cu plating heights near 278 microns in one particular trench (figure 9a). They also illustrated that frontside (top) planarity is maintained (figure 9b).



a) **b)**

Figure 9. Electroplated Cu surrounding chip: (a) seed under approach and (b) conformal seed over approach.

In the testing of other wafers with various trench widths, we note that the frontside gap between the chips and the template is less than five microns on average, showing that relatively planar interfaces are achievable. These wafer tests also show placement accuracy of better than 50 microns within an opening.

On the backside of the wafers in figure 9, the Cu functions as an electrical ground plane (relatively low potential) for chips to sink current and heat to. We notice that the backside Cu is not as smooth as it is on the frontside, but we are confident that we can shape the Cu via a chemical polishing or backside grinding technique.

3.5 Other Approaches/Materials to Embed Chips

One of our predetermined goals was to experiment with different materials and investigate their physical and chemical properties to better comprehend how to minimize material conflicts. One of these materials was SU-8, both a photo-definable resist and an irreversibly curable polymer, which we intended to use to encase the die. Analogous to a narrow tube, an individual trench is the container, whereby the SU-8 rises due to capillary action and coats the top surface of Silicon wafer #1. However, it is easier to control the plated Cu levels, where we know the plating rate based on the current density and surface area, than it is to force a drop of SU-8 to wick into a thin crack. This preference is one of the reasons we chose Cu over SU-8 as the binding material.

If SU-8 remains a part of the final structure, then hard baking or curing is imperative. One noteworthy property of SU-8 is its ability to cross-link or create intermolecular polymer bonds,

which are difficult to break apart and prevent further shaping of the chemically altered material. Once properly crosslinked, the material cannot be removed in acetone; other methods, such as chemical removal via DRIE etching, must be exercised. Exclusively thermally crosslinking demands hotplate exposure at a minimum temperature recommended by the manufacturer, a temperature at which the photoresist beneath started to visibly outgas. Hence, the SU-8 was deemed unsuitable for use.

While we did experiment with SU-8 in our process flow and observed that it bridges the gap between the chip edge and the sidewall (figure 10), its eventual drawbacks are its temperature sensitivities and incompatibilities with other parts of the process flow, ultimately rendering it inapplicable to our design concept. Electroplating Cu is a more robust solution.

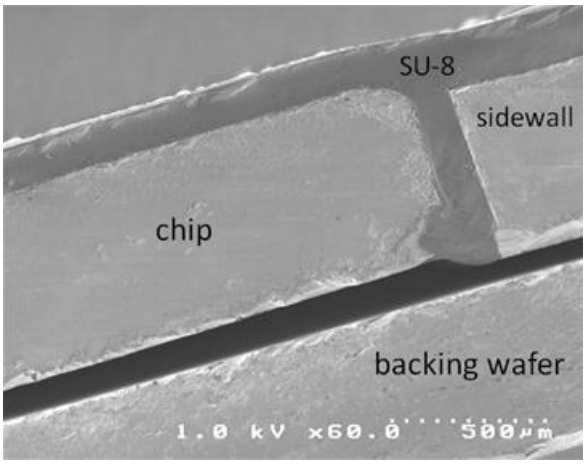


Figure 10. SU-8 wicking in between crevices.

4. Summary and Conclusions

By attempting to minimize material type incompatibilities and designing for a variety of Army-related applications, we have demonstrated a collection of capabilities in our first iterations of heterogeneous integration. For one, wafer-level integration of a Si blank die has been demonstrated. We established, refined, and proved the practicality of a linear microfabrication process flow. Additionally, we characterized the etch uniformity in the DRIE procedure, which is important for experimental repeatability. Difficulties arise from substrate size, thermal management/budget, and generalizability (making the platform as generic as possible while still applicable for most chip types). Finally, the trench layouts we designed are compatible with pick-and-place tools presently used in industry.

Future work includes the following:

- Evaluate compatibility of developed process with electronic devices on Si and alternative semiconductor substrate materials.
- Design and fabricate transmission lines and interconnects.
- Test electrical performance.
- Conformal deposition of Parylene or atomic layer deposition (ALD) insulators in the crevices to prevent shorting of a chip's substrate to the electroplated Cu.

While the process flow is still being advanced, we have made significant strides towards demonstrating a solid foundation for a heterogeneous integration to be built upon. Heterogeneous integration is practical, and contemporary prototypes have been built from the ground up to prove it.

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List of Symbols, Abbreviations, and Acronyms

ALD	atomic layer deposition
C_4F_8	octafluorocyclobutane
Cu	copper
DI	de-ionized
DRIE	deep reactive ion etching
DSP	double side polished
EBR	edge bead removal
H_2SO_4	sulfuric acid
PEB	post-exposure hard-baking
PECVD	plasma-enhanced chemical vapor deposition
RF	radio frequency
SEM	scanning electron microscopy
Si	silicon
SiO_2	silicon dioxide
SF_6	sulfur hexafluoride
TSVs	through-silicon-vias
UV	ultraviolet

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